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FISH & RICHARDSON, PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,996	BARNS ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-15 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-9 and 15,19-22* is/are rejected.

7)☒ Claim(s) *10-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-2, 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al (US 2002/0028555) in view of Thomas et al (US 2002/0019202)

Boyd discloses a method for fabrication a MOSFET. The method comprises the steps of:

depositing a polysilicon layer 52 on the semiconductor substrate, removing a portion of the polysilicon laver to form a high region and a low region (fig. 2A)

forming a silicide layer 36 over the semiconductor substrate (col 4, paragraph 0070)

removing a portion of the silicide laver 36 at a first rate and to remove the polvsilicon laver at a second rate by CMP wherein the first rate is higher than the second rate (col 4, paragraph 0072, fig. 2D shows all of the silicide layer 36 is removed after the CMP process while portion of polysilicon layer 52 still remains)

Unlike the instant claimed invention as per claim 1, Boyd fails to specifically disclose selecting chemical mechanical polishing parameters to remove the silicide layer at a higher rate than the polysilicon

Thomas, in a method for controlling of removal rate in CMP, discloses that the difference in removal rate is characterized by a parameter termed the selectivity ratio (col 1, paragraph 0005)

Since Boyd discloses removing a portion of the silicide laver 36 at a higher rate than polysilicon during the CMP process, one skilled in the art at the time the invention was made would have found it obvious to modify Boyd CMP process by selecting chemical mechanical polishing parameters to remove the silicide layer at a higher rate than the polysilicon as per Thomas because Thomas discloses that it is desirable for the removal rate of each layer to differ significantly from each other in order to reduce planarality and maintain the integrity od the semiconductor substrate during polishing (col 1, paragraph 0005)

Regarding claim 2, fig. 2A shows that the high region and the low region are formed before the silicide layer is formed and the silicide layer is removed from the high region (fig. 2D)

Regarding claim 5, Boyd discloses forming a dielectric layer 60 over the silicide layer (col 4, paragraph 0071), removing a portion of the dielectric layer to expose the silicide layer (col 4, paragraph 0072)

Regarding claims 6-7, Boyd discloses that the dielectric layer 60 comprises silicon dioxide and other insulator (col 4, paragraph 0071)

Regarding claim 8, Boyd discloses removing the dielectric layer by CMP (col 4, paragraph 0072)

3. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al (US 2002/0028555) in view of Thomas et al (US 2002/0019202) and further in view of Buynoski (US 6,194,299)

Boyd as modified by Thomas has been described above. Unlike the instant claimed invention as per claim 9, Boyd and Thomas fails to disclose the step of forming a top layer after forming the dielectric layer and removing a portion of the top layer before removing the portion of the dielectric layer

Buynoski discloses a method for fabricating of a low resistivity MOSFET comprises the step of forming a top layer 205 after forming the dielectric layer 204 and removing a portion of the top layer before removing the portion of the dielectric layer (col 3, lines 50-53; fig. 3)

One skilled in the art at the time the invention was made would have found it obvious to modify Boyd and Thomas by adding the step of forming a top layer after forming the dielectric layer and removing a portion of the top layer before removing the portion of

the dielectric layer in order to form a mask to etch/remove the dielectric layer as taught by Buynoski (col 3, lines 53-55)

4. Claims 15, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al (US 2002/0028555) in view of Thomas et al (US 2002/0019202)

Boyd discloses a method for fabrication a MOSFET. The method comprises the steps of:

forming a polysilicon feature on a semiconductor substrate having an intermediate gate dielectric layer 26 (col 3, paragraph 0059 ; fig. 1E)

depositing a first metal layer over the polysilicon feature; reacting the first metal layer with the polysilicon feature to form a metal silicide 36 (col 4, paragraph 0063)

depositing a dielectric layer 60 over the metal silicide and the semiconductor substrate (fig. 2C)

removing a portion of the dielectric layer over the metal silicide to expose a portion of the metal silicide 36 (col 4, paragraph 0072)

removing the portion of the metal silicide by chemical mechanical polishing (col 4, paragraph 0072), the metal silicide layer and the dielectric layer are removed by CMP at different polishing rates/first and second polishing rate (fig. 2C-2D)

removing the polysilicon feature 52 to create an opening in the gate dielectric layer (col 4, paragraph 0073; fig. 2E)

removing the gate dielectric laver (col 4, paragraph 0073; fig. 2E)

oxidizing the semiconductor substrate to form a new gate dielectric layer 62 (col 5, paragraph 0074)

Unlike the instant claimed invention as per claim 15, Boyd fails to explicitly disclose removing the metal silicide at a higher polishing rate than the polishing rate of the dielectric layer

Thomas, in a method for controlling of removal rate in CMP, discloses that the difference in removal rate is characterized by a parameter termed the selectivity ratio (col 1, paragraph 0005)

Since Boyd discloses removing a portion of the metal silicide (hard material) laver 36 at a different polishing rate than the dielectric (softer material) layer 60 during the CMP process, one skilled in the art at the time the invention was made would have found it obvious to modify Boyd CMP process by removing the silicide layer at a higher polishing rate than the dielectric in view of Thomas teaching because Thomas discloses that it is desirable for the removal rate of each layer to differ significantly from each other in order to reduce planarality and maintain the integrity of the semiconductor substrate during polishing (col 1, paragraph 0005)

Regarding claim 19, Boyd discloses filling the opening in the gate dielectric with metla layer 28 (col 5, paragraph 0077; fig. 2F)

6. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al (US 2002/0028555) in view of Thomas et al (US 2002/0019202)

Boyd discloses a method for fabrication a MOSFET. The method comprises the steps of:

depositing a polysilicon layer/material 52 on the semiconductor substrate, removing/patterning the polysilicon laver to form a high region and a low region (fig. 2A)

forming a silicide layer 36 in the high and low region (col 4, paragraph 0070, fig. 2B)

removing a portion of the silicide laver 36 from the high region at a first rate and to remove the polvsilicon laver at a second rate by CMP wherein the first rate is higher than the second rate (col 4, paragraph 0072, fig. 2D shows all of the silicide layer 36 in the high region is removed after the CMP process while portion of polysilicon layer 52 still remains

Unlike the instant claimed invention as per claim 20, Boyd fails to specifically disclose selecting chemical mechanical polishing parameters to remove the silicide layer at a higher rate than the polysilicon

Since Boyd discloses removing a portion of the silicide laver 36 at a higher rate than polysilicon during the CMP process, one skilled in the art at the time the invention was made would have found it obvious to modify Boyd CMP process by selecting chemical mechanical polishing parameters to remove the silicide layer at a higher rate than the polysilicon as per Thomas because Thomas discloses that it is desirable for the removal rate of each layer to differ significantly from each other in order to reduce planarality and maintain the integrity od the semiconductor substrate during polishing (col 1, paragraph 0005)

Regarding claim 21, fig. 2A of Boyd shows the high region comprises polysilicon layer 56

Regarding claim 22, fig. 2D of Boyd shows all of the silicide layer 36 in the high region is removed after the CMP process while portion of polysilicon layer/feature 52 still remains

Allowable Subject Matter

5. Claims 10-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 10, the cited prior art of record fails to disclose a method for fabricating a semiconductor structure comprises the step of forming a top layer comprises TiN after forming the dielectric layer, in combination with the rest of the limitations of claim 10. The closest cited prior art of Buynoski (US 6,194,299) discloses a method for fabricating of a low resistivity MOSFET comprises the step of forming a top layer 205 of photoresist after forming the dielectric layer 204 and removing a portion of the top layer before removing the portion of the dielectric layer (col 3, lines 50-53; fig. 3)

Response to Arguments

6. Applicant's arguments filed 2/17/2006 have been fully considered but they are not persuasive.

It is argued that Applicants disagree with the Examiner's assertion on pages 4 and 6 of the Office Action that Boyd, in paragraph 72, discloses removing a portion of the silicide layer at a higher rate than polysilicon during the CMP process and with the statement on page 6 of the Office Action that FIG. 217 of Boyd teaches the silicide layer having a higher removal rate than the polysilicon layer by showing "that all of the silicide layer 36 in the high region is removed after the CMP process while a portion of the polysilicon layer 52 still remains." because the structure depicted in FIG. 2D in no way whatsoever supports the assertion that the silicide layer is removed at a higher rate than the polysilicon layer. This argument is unpersuasive because of the following reasons: it is noted that according to the MPEP section 2111 [R-1] Claim Interpretation; Broadest Reasonable Interpretation : CLAIMS MUST BE GIVEN THEIR BROADEST REASONABLE INTERPRETATION

During patent examination, the pending claims must be "given *>their< broadest reasonable interpretation consistent with the specification." > In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000).

On page 7 of the instant specification, the applicants discloses "Referring also to Fig. 12, chemical mechanical polishing is continued to remove cobalt silicide region 46 from a top surface of polysilicon gate electrode 18. The chemical mechanical polishing is performed with a slurry providing a relatively low polishing rate for chemical mechanical

polysilicon 18, a relatively high for interlevel silicon dioxide 52, and a sufficiently high polishing rate for silicon nitride 50 and cobalt silicide 46 to achieve the structure illustrated in Fig. 12", Fig 12 shows that the gate polysilicon 18 is intact and the silicide 46 is completely removed after the CMP polishing step. Since Fig. 2D of Boyd also shows that the silicide 36 is completely removed while the polysilicon 52 remains intact after/as a result of the CMP polishing step, as similarly depicted in Fig. 12 of the instant specification, one skilled in the art would have found that it is obvious that Boyd silicide layer is removed at a higher rate than the polysilicon layer.

The applicants argue that the combination of Boyd and Thomas would fail to disclose the feature of claim 1 because there is nothing in Thomas that discloses or suggests selecting chemical mechanical polishing parameters to remove the silicide layer at a first rate and to remove the polysilicon layer at a second rate where the first rate is higher than the second rate. In response, Thomas is relied upon to teach that it is desirable for the removal rate of each layer to differ significantly from each other during polishing, and is not relied upon to teach to remove the silicide layer at a first rate and to remove the polysilicon layer at a second rate where the first rate is higher than the second rate. The primary reference of Boyd suggests that the silicide layer is removed at a first rate and the polysilicon layer is removed at a second rate where the first rate is higher than the second rate

7. Applicant's amendment necessitated the new ground(s) of rejection of claims 15, 19 presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
April 14, 2006